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FOR

CIRCUITS FOR RFID TAGS WITH MULTIPLE NON-INDEPENDENTLY DRIVEN RF PORTS

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FIELD OF THE INVENTION

[0001] The present invention is related to the field of Radio Frequency IDentification (RFID), and more specifically to devices, circuits, and methods for using multiple RF ports in RFID tag-to-reader communications.

BACKGROUND

[0002] Radio Frequency IDentification (RFID) tags can be used in many ways for locating and identifying objects that they are attached to. RFID tags are particularly useful in product-related and service-related industries for tracking large numbers of objects are being processed, inventoried, or handled. In such cases, an RFID tag is usually attached to individual items, or to their packages.

[0003] In principle, RFID techniques entail using a device called an RFID reader to interrogate one or more RFID tags. Interrogation is performed by the reader transmitting a Radio Frequency (RF) wave. A tag that senses the interrogating RF wave responds by transmitting back another RF wave, a process known as backscatter. The response may further encode a number stored internally in the tag. The response, and the number if available, is decoded by the reader, which thereby identifies, counts, or otherwise

interacts with the associated item. The number can denote a serial number, a price, a date, a destination, other attribute(s), any combination of attributes, and so on.

[0004] An RFID tag includes an antenna system, a radio section, a logical section, and a memory. Advances in semiconductor technology have miniaturized the electronics so much that an RFID tag can generate the backscatter while powered by only the RF signal it receives, enabling some RFID tags to operate without a battery.

[0005] It is desirable that the antenna system have components such that it is able to sense many possible types of interrogating RF waves, and from many possible directions, regardless of the orientation of the tag. For example, some RFID tags are provided with antennas that are suitable for sensing RF waves of different polarization. It has been known to have a system of two antennas, driving them independently of each other to generate two backscatter signals. Such is taught, for example in Patent Application US 2002/0167405A1, published on 2002-11-14 to Shanks et al. Independent driving, however, requires more circuitry and more power than single antenna systems.

BRIEF SUMMARY

[0006] The invention improves over the prior art. Briefly, the invention drives different points of an antenna system of an RFID tag non-independently. The invention provides devices and circuits that may be used for RFID tags, and which have multiple non-independent RF ports. The invention also provides methods for driving such RF ports non-independently from each other. These in turn may drive corresponding points of the antenna system of the RFID tag. The invention is particularly advantageous where different antenna points correspond to different polarizations.

[0007] In one embodiment, two RF ports are driven by a common modulating signal, for example to enable a single modulator to be used for generating backscatter in two polarizations.

[0008] In another embodiment, two RF ports are driven by either separate modulating signals, or by the common modulating signal as above. Further, the ports may be coupled and uncoupled together, responsive to a control signal. As yet another option, the control signal may be the same as one or both of these modulating signals.

[0009] The invention further provides for an RFID antenna driver implemented in a semiconductor device with non-independent RF ports. These and other features and advantages of the invention will be better understood from the specification of the invention, which includes the following Detailed Description and accompanying Drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The following Detailed Description proceeds with reference to the accompanying Drawings, in which:

FIGURE 1 is a view of an RFID tag with a first sample type of antenna system;

FIGURE 2 is a view of another RFID tag with a second sample type of antenna system;

FIGURE 3 is a hybrid circuit diagram of a circuit for an RFID tag, where a common modulating signal drives different RF ports;

FIGURE 4A is a hybrid circuit diagram of another circuit for an RFID tag, where a control signal controls coupling and uncoupling two RF ports;

FIGURE 4B is a hybrid circuit diagram of a possible more detailed embodiment of the circuit of FIGURE 4A;

FIGURE 5 is a hybrid circuit diagram of yet another circuit for an RFID tag, where two RF ports are driven by a common modulating signal, and further where the modulating signal controls coupling and uncoupling of the two RF ports;

FIGURE 6 is a layout for implementing components of the hybrid circuit diagram of FIGURE 5 in a semiconductor device;

FIGURE 7 illustrates a first optimized layout in abstract form for implementing the structure of FIGURE 6 in a compact and efficient fashion;

FIGURE 8 illustrates a second optimized layout in abstract form for implementing the structure of FIGURE 6 in a compact and efficient fashion;

FIGURE 9 illustrates a particular implementation of a unit tile of the optimized layout of a variant of FIGURE 8; and

FIGURE 10 is a flowchart illustrating a method, all according to embodiments of the present invention.

DETAILED DESCRIPTION

[0011] The present invention is now described. While it is disclosed in its preferred form, the specific embodiments of the invention as disclosed herein and illustrated in the drawings are not to be considered in a limiting sense. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Indeed, it should be readily apparent in view of the present description that the invention may be modified in numerous ways. Among other things, the present invention may be embodied as devices, circuits, methods, and so on. The following detailed description is, therefore, not to be taken in a limiting sense.

[0012] As used herein, the symbol n+ indicates an n-doped semiconductor material typically having a doping level of n-type dopants on the order of 10^{21} atoms per cubic centimeter. The symbol n- indicates an n-doped semiconductor material typically having a doping level on the order of 10^{17} atoms per cubic centimeter. The symbol p+ indicates a p-doped semiconductor material typically having a doping level of p-type dopants on the order of 10^{21} atoms per cubic centimeter. The symbol p- indicates a p-doped semiconductor material typically having a doping level on the order of 10^{17} atoms per cubic centimeter. Those of ordinary skill in the art will now realize that the devices described herein may be formed on a conventional semiconductor substrate or they may as easily be formed as a thin film transistor (TFT) above the substrate, or in silicon on an insulator (SOI) such as glass (SOG), sapphire (SOS), or other substrates as known to those of ordinary skill in the art. Such persons of ordinary skill in the art will now also

realize that a range of doping concentrations around those described above will also work. Essentially, any process capable of forming pFETs and nFETs will work. Doped regions may be diffusions or they may be implanted.

[0013] As has been mentioned, the invention drives different points of an antenna system of an RFID tag non-independently. The invention is now described in more detail.

[0014] The invention may be used with RFID tags having many types of antenna systems. Two such systems are described below as a way of example, but not of limitation.

[0015] FIGURE 1 is a view of a sample RFID tag 110 that may be used with the invention. Tag 110 is formed on a substrate 115, which does not conduct. Tag 110 has an antenna system that includes a rectangular conductive plate 130. Preferably it also includes a complementary matching plate (not shown) on the opposite of substrate 115.

[0016] Conductive plate 130 has two main directions, one along horizontal axis 132 and one along vertical axis 134. The two directions result in two resonant modes for plate 130. The geometry of plate 130 is especially useful if the interrogating RF wave is circularly polarized.

[0017] Backscatter signals may be generated by a circuit that resides on a chip (not shown in FIGURE 1), and connected to the antenna system. The circuit receives an interrogating RF signal through the antenna during a receive phase, and drives the antenna system accordingly, during a transmit phase. Driving may be performed at points on antenna plate 130 that are optimal for the prevailing resonant modes. Such points may, for example, be at antenna point A1 on axis 132 for a first polarization, and at antenna point A2 on axis 134 for a second polarization. Of course, driving may be with respect to a reference, which in turn may be applied to a complementary point of the complementary matching plate. For driving the antenna, wires (not shown) couple the circuit with antenna points A1, A2, and also with their complementary points on the complementary matching plate.

[0018] FIGURE 2 is a view of another sample RFID tag 210 that may be used with the invention. Tag 210 is formed on a non-conducting substrate 215. Two substantially collinear antenna segments ANT14, ANT15 form a linear antenna for a first dominant polarization direction, while another two substantially collinear antenna segments ANT24, ANT25 form a second linear antenna for a second dominant polarization direction. The geometry of these antennas is especially useful if the interrogating RF wave is linearly polarized. Such a wave will generate a component in each of the linear antennas.

[0019] A chip 250 on tag 210 includes a circuit, which generates backscatter. Chip 250 drives at least one of the antenna segments, such as segment ANT14. Driving may be

with respect to a reference, which in turn may be applied to drive the complementary antenna segment ANT15. For a first polarization, driving is at an antenna point A1 of segment ANT14, and optionally also segment ANT15. For a second polarization, driving is at an antenna point A2 of segment ANT24, and optionally also segment ANT25.

[0020] Regardless of what type antenna system is employed by the RFID tag, the invention provides driving RF ports of a circuit, which in turn drive the points of the antenna system. Driving the RF ports may be implemented in a number of ways. One such way is to drive the RF ports with a common modulation signal. Another such way is to alternately couple and uncouple the RF ports together, according to a control signal. During the times when the RF ports are uncoupled, they could be operating either from a common, or from different modulating signals. In one embodiment, the control signal is the same as one or both of the modulating signals, and so on. Examples of such ways are discussed in more detail below.

[0021] FIGURE 3 shows a hybrid circuit diagram of a circuit 350 for an RFID tag 310. Tag 310 may be implemented with an antenna system configured so that it receives RF signals, and can retransmit different polarizations by being driven at different antenna points A1, A2.

[0022] Circuit 350 may advantageously be provided as an integrated circuit. This will result in economical manufacture, and small size. A number of its components are provided in block 380, labeled OTHER CIRCUITRY.

[0023] Circuit 350 includes a first RF port P31, which is coupled to first antenna point A1 when the RFID tag is assembled. Circuit 350 also includes a second RF port P32, which is coupled to second antenna point A2 when the RFID tag is assembled. RF ports P31, P32 are also known as ports. Coupling to the antenna points may be by wire, bump soldering, or other ways known in the art.

[0024] Circuit 350 moreover includes a first modulating switch T31. Switch T31 is configured to selectively couple and uncouple port P31 to a first reference voltage RV31. Coupling and uncoupling is performed responsive to a modulating signal MS3. Reference voltage RV31 may be optionally further coupled to another RF port (not shown) complementary to port P31, and which would in turn be coupled to another antenna point (not shown) that is complementary to point A1.

[0025] Circuit 350 furthermore includes a second modulating switch T32. Switch T32 is configured to selectively couple and uncouple port P32 to a second reference voltage RV32. Coupling and uncoupling is performed responsive to modulating signal MS3. Reference voltage RV32 may be optionally further coupled to another RF port (not shown) complementary to port P32, and which would in turn be coupled to another antenna point (not shown) that is complementary to point A2. In addition, reference voltage RV32 may be equivalent to reference voltage RV31, such as by being coupled with it. Reference voltages RV31 and RV32 may further be a common ground.

[0026] Modulating signal MS3 is preferably a signal that alternates, and wherein its alternation causes coupling and uncoupling. The alternation thus affects the impedance of the antenna system, which in turn causes backscatter.

[0027] It will be observed that switches T31, T32 are driven by a common modulating signal MS3, in other words a single modulating signal. Accordingly, in this embodiment of the invention a single modulator may be used to generate signal MS3 that drives the two different ports P31, P32. The single modulator may have components in functional block 380. Having a single modulator results in less occupied space than where two modulators are provided.

[0028] Switches T31 and T32, as well as other switches in this description, may be made from switching circuits such as transistors. Such transistors include MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) that include nFETs and pFETs, jFETs (junction FETs), BJTs (bipolar junction transistors), MESFETs (MEtal Semiconductor FETs), FinFETs (fin FETs), HBTs (Heterojunction Bipolar Transistors), IGFETs (Insulated Gate Transistors), TFTs (Thin Film Transistors), and so on. In the event they are made as MOSFET transistors, modulating signal MS3 may be applied directly to their gates.

[0029] FIGURE 4A is a hybrid circuit diagram of a circuit 450-A for RFID tag 310. Circuit 450-A may be substituted in lieu of circuit 350 in FIGURE 3, and antenna points

of tag 310 (such as A1, A2) would be coupled instead to respective ports of circuit 450-A (such as P41, P42).

[0030] Circuit 450-A may be implemented in a number of ways, and a number of its components may be implemented in block 480-A. Circuit 450-A further includes a connecting switch TC4. Switch TC4 selectively couples and uncouples port P41 to port P42. Coupling and uncoupling is performed responsive to a control signal CS4.

[0031] It is preferred that switch TC4 be made from a MOSFET transistor, in which case control signal CS4 may be applied directly to the gate of the MOSFET transistor.

[0032] FIGURE 4B is a hybrid circuit diagram of a possible more detailed embodiment of the circuit of FIGURE 4A. In addition to what is shown for circuit 450-A, circuit 450-B includes a first modulating switch T41. Switch T41 is configured to selectively couple and uncouple port P41 to a first reference voltage RV41. Coupling and uncoupling is performed responsive to a modulating signal MS41. Reference voltage RV41 may be optionally further coupled to another RF port (not shown) complementary to port P41, and which would in turn be coupled to another antenna point (not shown) that is complementary to point A1.

[0033] Circuit 450-B furthermore includes a second modulating switch T42. Switch T42 is configured to selectively couple and uncouple port P42 to a second reference voltage RV42. Coupling and uncoupling is performed responsive to modulating signal

MS42. Reference voltage RV42 may be optionally further coupled to another RF port (not shown) complementary to port P42, and which would in turn be coupled to another antenna point (not shown) that is complementary to point A2.

[0034] It is preferred that switches T41 and T42 be made from MOSFET transistors, in which case modulating signals MS41, MS42 may be applied directly to the gates of the MOSFET transistors, as shown. In addition, reference voltage RV41 may be equivalent to reference voltage RV42, such as by being coupled with it. Reference voltages RV41 and RV42 may further be a common ground.

[0035] Modulating signals MS41 and MS42 are generated from block 480-B. While RF port P41 is coupled, via switch TC4, to RF port P42, modulating signal MS41 is preferably the same as modulating signal MS42. But while RF port P41 is not coupled to RF port P42, modulating signal MS41 may be the same or different than modulating signal MS42. Alternately, modulating signal MS41 may have some similar and some different aspects than modulating signal MS42. For example, modulating signal MS41 may alternate at a different frequency than modulating signal MS42. Or they may alternate at the same frequency, but with a different phase. Or one of modulating signals MS41 and MS42 may be modulating, while the other one might not.

[0036] FIGURE 5 is a hybrid circuit diagram of a circuit 550 for RFID tag 310. Circuit 550 may be substituted in lieu of circuit 350 in FIGURE 3, and antenna points of tag 310

(such as A1, A2) would be coupled instead to respective ports of circuit 550 (such as P51, P52).

[0037] Circuit 550 may be implemented in a number of ways, such as a semiconductor integrated circuit and so on. In addition, a number of its components may be implemented in block 580, which generates a modulating signal MS5.

[0038] Circuit 550 includes a first modulating switch T51. Switch T51 is configured to selectively couple and uncouple port P51 to a ground, which may be optionally further coupled to an antenna point that is complementary to point A1. Coupling and uncoupling is performed responsive to modulating signal MS5. Circuit 550 furthermore includes a second modulating switch T52. Switch T52 is configured to selectively couple and uncouple port P52 to the ground, which may be optionally further coupled to an antenna point that is complementary to point A2. Coupling and uncoupling is performed responsive to modulating signal MS5.

[0039] Circuit 550 additionally includes a connecting switch TC5. Switch TC5 selectively couples and uncouples port P51 to port P52. Coupling and uncoupling is performed responsive to modulating signal MS5.

[0040] It will be appreciated that the example of FIGURE 5 is a special case of what is shown in FIGURE 3, FIGURE 4A, and FIGURE 4B. For circuit 550, the modulating

signal for first switch T51 is the same as for second switch T52, and further the same as the control signal for switch TC5.

[0041] It is preferred that switches T51, T52, TC5 be made from MOSFET transistors, in which case a modulating signal MS5 may be applied directly to the gates of the MOSFET transistors, as shown.

[0042] In a further aspect of the invention, switches T51, T52, TC5 are provided as a single semiconductor device. Such is described below in more detail.

[0043] FIGURE 6 is a layout for implementing switches T51, T52, TC5 of FIGURE 5 in a semiconductor device. An area 610 in a substrate 600 is separated vertically from a conductive layer 612 by an insulating layer (not shown). The insulating layer may be made from oxide, and conductive layer 612 from polycrystalline or metallic material.

[0044] When implanted with dopants, areas 610 and 612 define three implants, where layer 612 does not cover area 610. Substrate 600 may be made from p-type silicon, in which case the dopants are advantageously n-type. (Alternately, substrate 600 may be made from n-type silicon, in which case the dopants are advantageously p-type.) Contacts are then provided for the implants. The geometry thus defines a source S6, shown at the contact, and two drains D61, D62, also shown at the contact.

[0045] It will be recognized that transistor T51 of FIGURE 5 results as a MOSFET between source S6 and drain D61. Indeed, a first channel CH1 is defined between source S6 and drain D61. Further, transistor T52 results as a MOSFET between source S6 and drain D62, as a second channel CH2 is defined between source S6 and drain D62. Further, conductive layer 612 operates as a common gate to transistors T51 and T52, essentially combining transistors T51 and T52 into a single device.

[0046] Moreover, area 620 in substrate 600 is separated vertically from a gate layer 622 by an insulating layer (not shown). When implanted with dopants, areas 620 and 622 define a fourth implant SC and a fifth implant DC, on which contacts may be deposited. Implant SC may be coupled to implant D1 via conductor 642, and implant DC may be coupled to implant D2 via conductor 644.

[0047] In each case, the dopant density and other parameters have preferably the needed values to form MOSFET transistors. This way, connecting transistor TC5 of FIGURE 5 results as a MOSFET between source SC and drain DC. Indeed, a third channel CHC is defined between the implant SC and implant DC, and gate layer 622 is over it.

[0048] The device of FIGURE 6 may be used for implementing switches T51, T52, TC5 of FIGURE 5. Indeed, source SC may be coupled with RF port P51 using conductor 652, and drain DC may be coupled with RF port P52 using conductor 654. Moreover,

conductive layer 612 can be coupled with gate layer 622, in which case it also switches transistor TC5.

[0049] FIGURE 7 and FIGURE 8 illustrate abstract layouts 700, 800, for implementing the structure of FIGURE 6 in a compact and efficient fashion. It will be appreciated that these are especially useful if any one structure has insufficient driving capacity.

[0050] In FIGURE 7, source regions S7 are located diagonally, in a checkerboard fashion. First and second drain regions D71, D72 are located alternatingly, in the spaces left between source regions S7. A common gate 712 has a minimum unit tile 714 that is cross-shaped.

[0051] In FIGURE 8, source regions S8 are in a line, while first and second drain regions D71, D72 are also in a line but alternate. A common gate 812 has a minimum unit tile 814 that is T-shaped, here shown inverted. In a variant of layout 800, gate 812 is interrupted in horizontal lines, between neighboring source regions S8.

[0052] In both FIGURE 7 and FIGURE 8, like regions are connected together by suitable conductors, and so on. Further, each is made by repeating the structure of a unit tile.

[0053] FIGURE 9 shows a unit tile of the variant of layout 800. The unit tile for the layout of FIGURE 700 is analogous.

[0054] In a substrate 900, an area 910 is separated vertically from a conductive layer 912 by an insulating layer (not shown). Layer 912 is T-shaped, here shown inverted. The insulating layer may be made from oxide, and conductive layer 912 from polycrystalline or metallic material.

[0055] When implanted with dopants, areas 910 and 912 define in substrate 900 three regions where layer 912 does not cover area 910. Substrate 900 may be made from p-type silicon, in which case the dopants are advantageously n-type. (Alternately, substrate 600 may be made from n-type silicon, in which case the dopants are advantageously p-type.) Contacts are then provided for the regions. The geometry thus defines two drain regions D91, D92, and a source region with one or more contacts S9.

[0056] It will be recognized that a very compact device is thus generated for an RFID tag, that can drive the two RF ports non-independently. Transistor T51 of FIGURE 5 results as a MOSFET between source S9 and drain D91, as a channel DR1 is defined in substrate 900 between source S9 and drain D91. Additionally, transistor T52 results as a MOSFET between source S9 and drain D92, as a channel DR2 is defined in substrate between source S9 and drain D92. Moreover, connecting transistor TC5 results as a MOSFET between drain D91 and drain D92, as a connecting channel DRC is defined in substrate 900 between drain D91 and drain D92. Conductive layer 912 operates as a common gate for all three transistors T51, T52, TC5. Indeed, a voltage on it affects

concurrently all channels DR1, DR2, DRC. Drain regions D1, D2 may be electrically coupled with output RF ports P51, P52, via conductors 952, 954, respectively.

[0057] FIGURE 10 is flowchart 1000 illustrating a method according to an embodiment of the invention. The method of flowchart 1000 may be practiced by different embodiments of the invention, including but not limited to tags 110, 210, 310, chip 250, and circuits 350, 450-A, 450-B, and 550. Furthermore, many of the terms of FIGURE 10 draw their meaning from the description above.

[0058] At block 1010, a first signal is received at a first antenna port. At next block 1020, a first modulating signal is generated in response to the first received signal. At a next block 1030, the first port is coupled and uncoupled to a first reference voltage responsive to the first modulating signal. At a next block 1040, a second port is coupled and uncoupled to a second reference voltage responsive to a second modulating signal, which may be the same as the first modulating signal or not. At optional next block 1050, the first port is coupled and uncoupled to the second port, responsive to a control signal. The control signal may be the same as the first modulating signal.

[0059] Numerous details have been set forth in this description, which is to be taken as a whole, to provide a more thorough understanding of the invention. In other instances, well-known features have not been described in detail, so as to not obscure unnecessarily the invention.

[0060] The invention includes combinations and subcombinations of the various elements, features, functions and/or properties disclosed herein. The following claims define certain combinations and subcombinations, which are regarded as novel and non-obvious. Additional claims for other combinations and subcombinations of features, functions, elements and/or properties may be presented in this or a related document.